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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,525	01/06/2004	Mitsuyasu Ohta	60188-725	3295

7590 12/12/2007

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2117	

MAIL DATE	DELIVERY MODE
12/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/751,525	OHTA ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/18/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-17 and 19-20 are pending in the present application.

Information Disclosure Statement

The Information Disclosure Statement provided to the Office on August 18, 2004 has been reviewed and re-signed to indicate acknowledgement of U.S. Patent No. 5,258,985. A copy of this document has been provided with this office action.

Response to Arguments

Applicant's arguments with respect to claims 1-17 and 19-20 have been considered but are moot in view of the new ground(s) of rejection.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-17 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-10 of U.S. Patent No. 6,708,301. Although the conflicting claims are not identical, they are not patentably distinct from each other because the limitations of claim 1 of the present application are fully contained within the U.S. Patent as shown below.

Claim 1 of the present application reads: A functional block for an integrated circuit, comprising a test data output circuit for outputting test data responsive to a control signal indicating a test data transmission state.

Claim 1 of the U.S. Patent reads: A semiconductor integrated circuit comprising: a first functional block including a test data output circuit for outputting test data responsive to a first control signal indicating a test data transmission state; a second functional block for the integrated circuit, including a decision result output circuit for receiving the test data responsive to a second control signal indicating a test data reception state, deciding whether the test data received is correct or erroneous, and outputting a result of the decision; a test control output section for outputting the first and second control signals to the first and second functional blocks for integrated circuit, respectively; and a test result output circuit for receiving a decision result signal from the decision result output circuit and outputting the received decision result signal as a test result signal.

Claims 8-10 of the U.S. Patent read as follows; A method for testing a semiconductor integrated circuit, the semiconductor integrated circuit comprising: a first

functional block including a test data output circuit for outputting test data responsive to a first control signal indicating a test data transmission state; a second functional block for the integrated circuit, including a decision result output circuit for receiving the test data responsive to a second control signal indicating a test data reception state, deciding whether the test data received is correct or erroneous, and outputting a result of the decision; a third functional block for the integrated circuit, including a testing standby circuit for blocking the output of an output signal responsive to a third control signal indicating a testing standby state; a test control output section for outputting the first, second and third control signals to the first, second and third functional blocks for the integrated circuit, respectively; and a test result output circuit for receiving a decision result signal from the decision result output circuit and outputting the received decision result signal as a test result signal, the method comprising: a test data transmitting step for making the test control output section output the first control signal to make the test data output circuit of the first functional block for the integrated circuit output the test data; a test data receiving step for making the test control output section output the second control signal to make the decision result output circuit of the second functional block for the integrated circuit, which is connected to the first functional block for the integrated circuit, receive the test data; a testing standby step for making the test control output section output the third control signal to make the testing standby circuit of the third functional block for the integrated circuit, which is connected to the first functional block for the integrated circuit, block the output; and a test result reading step for reading the test result from the test result output circuit.

9. The method for testing a semiconductor integrated circuit of claim 8, wherein the test data output circuit includes a plurality of output signal lines enabling parallel output, and the test data transmitting step includes: an initial signal line dividing step for dividing the output signal lines into two groups and outputting the test data through the output signal lines such that the respective groups divided have mutually different values, which change from one value into the other; a signal line dividing step for dividing each said group into two groups and outputting the test data through the output signal lines such that the respective groups divided have mutually different values, which change from one value into the other; and a testing step for repeatedly performing the signal line dividing step until the output signal line belonging to each said group is no longer divisible.

10. A method for designing a semiconductor integrated circuit using a plurality of functional blocks for the integrated circuit, each said functional block for the integrated circuit performing a predetermined function of a logic or memory circuit, the method comprising: a functional block designing step for introducing, into each of the functional blocks for the integrated circuit, at least one of: a test data output circuit for outputting test data responsive to a control signal indicating a test data transmission state; a decision result output circuit for receiving the test data responsive to a control signal indicating a test data reception state, deciding whether the test data received is correct or erroneous, and outputting a result of the decision; and a testing standby circuit for blocking the output of an output signal responsive to a control signal indicating a testing standby state; a functional block library forming step for forming a library of functional

blocks by registering the functional blocks for the integrated circuit, which have been made in the functional block designing step, at the library; and a functional block selecting step for selecting such a functional block for the integrated circuit as enabling a desired semiconductor integrated circuit from the functional blocks for the integrated circuit that are included in the library of functional blocks.

Claim 2 of the present application reads; The functional block for an integrated circuit of Claim 1, characterized in that the test data output circuit includes a plurality of output signal lines enabling parallel output, and outputs the test data such that an adjacent pair of the output signal lines have mutually different values. However these limitations are substantially included in claim 9. Claim 9 recites 'respective groups instead of adjacent pairs. This is an obvious variation. The remaining dependent claims are also fully covered within the claims of the U.S. Patent with minor obvious variations.

Claim 3 of the present application reads; The functional block for an integrated circuit of Claim 1, characterized in that the test data output circuit outputs the test data changing from one value into the other. Test data changing is covered in the context of claim 9 of the U.S. Patent

As such, the remaining dependent claims will not be specifically pointed out although applicant is invited to call and discuss these limitations with the examiner if there are questions which may be better clarified by conducting an interview.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt
Primary Examiner 12/7/04
Art Unit 2117